IN THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Original) A mixer circuit, comprising:

a mixer including an IF signal output load portion, an LO signal processing portion, and an RF signal processing portion, which are connected in cascade connection between a power supply and a ground;

an RF signal supplier for supplying an RF signal to the RF signal processing portion;

an LO signal supplier for supplying an LO signal to the LO signal processing portion; and

at least a bypass current supply portion for bypassing a bias current of the LO signal processing portion.

2. (Original) A mixer circuit as defined in Claim 1, where the bypass current supply portion is connected in parallel with the LO signal processing portion.

3. (Original) A mixer circuit as defined in Claim 1, where the bypass current supply portion additionally supplies a bias current only to the RF signal processing portion.

4. (Original) A mixer circuit as defined in Claim 1, where the bypass current supply portion includes a first bypass current source for additionally supplying a bias current only to the RF signal processing portion, and a second bypass current source for additionally supplying a bias current only to the IF signal output load portion.

5. (Original) A mixer circuit comprising:

a single balanced mixer including an IF signal output load portion, an LO signal processing portion, and an RF signal processing portion, which are connected in cascade connection between a supply voltage and a ground;

an RF signal supplier for supplying an RF signal to the RF signal processing portion;

an LO signal supplier for supplying an LO signal to the LO signal processing portion;

at least one bypass current supply portion for bypassing a bias current of the LO signal processing portion; and

said IF signal output load portion including a first load resistor having an end connected to the power supply and another end connected to a first IF output terminal, and a second load resistor having an end connected to the power supply and another end connected to a second IF output terminal;

the RF signal processing portion including an RF transistor having a source terminal connected to the ground;

said LO signal processing portion including a first LO transistor having a source terminal connected to a drain terminal of the RF transistor and a drain terminal connected to the first IF output terminal, and a second LO transistor having a source terminal connected to the drain terminal of the RF transistor and a drain terminal connected to the second IF output terminal.

6. (Original) A mixer circuit as defined in Claim 5, where the bypass current supply portion includes a first bypass current source which is connected in parallel with the first LO transistor between the first IF output terminal and the drain terminal of the RF transistor, and a second bypass current source which is connected in parallel with the second LO transistor between the second IF output terminal and the drain terminal of the RF transistor.

7. (Original) A mixer circuit as defined in Claim 5, where the bypass current supply portion includes a first bypass current source for additionally supplying a bias current only to the RF transistor, which is connected between the power supply and the drain terminal of the RF transistor.

8. (Original) A mixer circuit as defined in Claim 5, where the bypass current supply portion includes a first bypass current source for additionally supplying a bias current only to the RF transistor, which is connected between the supply voltage and the drain terminal of the RF

transistor, a second bypass current source for additionally supplying a bias current only to the first load resistor, which is connected between the first IF output terminal and the ground, and a third bypass current source for additionally supplying a bias current only to the second load resistor, which is connected between the second IF output terminal and the ground.

9. (Original) A mixer circuit, comprising:

a double balanced mixer including an IF signal output load portion, an LO signal processing portion, and an RF signal processing portion, which are connected in cascade connection between a power supply and a ground;

an RF signal supplier for supplying an RF signal to the RF signal processing portion; an LO signal supplier for supplying an LO signal to the LO signal processing portion;

at least one bypass current supply portion for bypassing a bias current of the LO signal processing portion; and

the IF signal output load portion including a first load resistor having an end connected to the power supply and another end connected to a first IF output terminal, and a second load resistor having an end connected to the power supply and another end connected to a second IF output terminal;

the RF signal processing portion including a first RF transistor and a second RF transistor each having a source terminal connected to the ground; and

the LO signal processing portion including a first LO transistor having a source terminal connected to a drain terminal of the first RF transistor and a drain terminal connected to the first IF output terminal, a second LO transistor having a source terminal connected to the drain terminal of the first RF transistor and a drain terminal connected to the second IF output terminal, a third LO transistor having a source terminal connected to a drain terminal of the second RF transistor and a drain terminal connected to the first IF output terminal, and a fourth LO transistor having a source terminal is connected to the drain terminal of the second RF transistor and a drain terminal connected to the second IF output terminal.

10. (Original) A mixer circuit as defined in Claim 9, where the bypass current supply portion includes a first bypass current source which is connected in parallel with the first LO transistor

between the first IF output terminal and the drain terminal of the first RF transistor, a second bypass current source which is connected in parallel with the second LO transistor between the second IF output terminal and the drain terminal of the first RF transistor, a third bypass current source which is connected in parallel with the third LO transistor between the first IF output terminal and the drain terminal of the second RF transistor, and a fourth bypass current source which is connected in parallel with the fourth LO transistor between the second IF output terminal and the drain terminal of the second RF transistor.

11. (Original) A mixer circuit as defined in Claim 9, where the bypass current supply portion includes a first bypass current source which is connected in parallel with the first LO transistor between the first IF output terminal and the drain terminal of the first RF transistor, and a second bypass current source which is connected in parallel with the fourth LO transistor between the second IF output terminal and the drain terminal of the second RF transistor.

12. (Original) A mixer circuit as defined in Claim 9, the bypass current supply portion includes a first bypass current source for additionally supplying a bias current only to the first RF transistor, which is connected between the power supply and the drain terminal of the first RF transistor, and a second bypass current source for additionally supplying a bias current only to the second RF transistor, which is connected between the supply voltage and the drain terminal of the second RF transistor.

13. (Original) A mixer circuit as defined in Claim 9, where the bypass current supply portion includes a first bypass current source for additionally supplying a bias current only to the first RF transistor, which is connected between the power supply and the drain terminal of the first RF transistor, a second bypass current source for additionally supplying a bias current only to the second RF transistor, which is connected between the supply voltage and the drain terminal of the second RF transistor, a third bypass current source for additionally supplying a bias current only to the first load resistor, which is connected between the first IF output terminal and the ground, and a fourth bypass current source for additionally supplying a bias current only to the second load resistor, which is connected between the second IF output terminal and the ground.

14. (Currently Amended) A mixer circuit as defined in ~~any of Claims 1, 5, and 9~~ Claim 1, where the first to fourth bypass current sources include a bias circuit having a bias voltage output terminal, and a current source transistor having a gate terminal connected to the bias voltage output terminal.

15. (Currently Amended) A mixer circuit as defined in ~~any of Claims 1, 5, and 9~~ Claim 1, the mixer, the single balanced mixer, and the double balanced mixer are respectively constituted by an MOS transistor.

16. (Currently Amended) A mixer circuit as defined in ~~any of Claims 1, 5, and 9~~ Claim 1, where the mixer circuit is one which is employed in a receiving system according to a direct conversion system, or a receiving system according to a Low IF system.

17. (New) A mixer circuit as defined in any of Claims 1, 5, and 9 Claim 5, where the first to fourth bypass current sources include a bias circuit having a bias voltage output terminal, and a current source transistor having a gate terminal connected to the bias voltage output terminal.

18. (New) A mixer circuit as defined in any of Claims 1, 5, and 9 Claim 9, where the first to fourth bypass current sources include a bias circuit having a bias voltage output terminal, and a current source transistor having a gate terminal connected to the bias voltage output terminal.

19. (New) A mixer circuit as defined in any of Claims 1, 5, and 9 Claim 5, the mixer, the single balanced mixer, and the double balanced mixer are respectively constituted by an MOS transistor.

20. (New) A mixer circuit as defined in any of Claims 1, 5, and 9 Claim 9, the mixer, the single balanced mixer, and the double balanced mixer are respectively constituted by an MOS transistor.

21. (New) A mixer circuit as defined in any of Claims 1, 5, and 9 Claim 5, where the mixer circuit is one which is employed in a receiving system according to a direct conversion system, or a receiving system according to a Low IF system.

22. (New) A mixer circuit as defined in any of Claims 1, 5, and 9 Claim 9, where the mixer circuit is one which is employed in a receiving system according to a direct conversion system, or a receiving system according to a Low IF system.